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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,961	09/26/2003	Glenn J. Leedy	ELM-2 CONT. 4	9439

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EXAMINER	
LEWIS, MONICA	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,961	LEEDY, GLENN J.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-115* is/are pending in the application.

4a) Of the above claim(s) *89-94,96-105 and 115* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *88,95,106-109 and 111-114* is/are rejected.

7)☒ Claim(s) *110* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/26/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the election filed May 26, 2005.

Election/Restrictions

2. Applicant's election with traverse of Embodiment III in the reply filed on 5/26/05 is acknowledged. However, applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, therefore, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The requirement is still deemed proper and is therefore made FINAL.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim 88 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,563,224. Although the conflicting claims are not identical, they are not patentably distinct from each other.

In regards to claim 88, Leedy discloses the following:

a) a first substrate (See Claim 1);

b) a second substrate bonded to the first substrate (See Claim 1); and

c) conductive paths formed between the first substrate and the second substrate, wherein the second substrate is a thinned substrate having circuitry formed thereon (See Claim 1).

Note: The differences between Applicant's claim 88 and Leedy's claim 1 are as follows:

Applicant's claim 88

a) An integrated circuit structure comprising:

Leedy's claim 1

a) An integrated **memory** circuit structure comprising:

Applicant's claim 88

a) conductive paths **formed** between

Leedy's claim 1

a) conductive paths between.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 88 and 95 are being rejected under 35 U.S.C. 102(b) as being anticipated by Faris (U.S. Patent No. 5,786,629).

In regards to claim 88, Faris discloses the following:

a) a first substrate (7 and 10) (For Example: See Figure 4);

b) a second substrate (7 and 10) bonded (17) to the first substrate (For Example: See Figure 4); and

c) conductive paths formed between the first substrate and the second substrate, wherein the second substrate is a thinned substrate having circuitry formed thereon (For Example: See Figure 4, Column 4 Lines 57-67, Column 5 Lines 8-13, Column 6 Lines 12-17, Column 7 Lines 45-48).

In regards to claim 95, Faris discloses the following:

a) at least one additional thinned substrate having circuitry formed thereon (For Example: See Figure 4, Column 4 Lines 57-67, Column 5 Lines 8-13, Column 6 Lines 12-17, Column 7 Lines 45-48);

b) a first of said at least one additional thinned substrate being bonded to the second substrate and any additional thinned substrates being bonded to the directly adjacent thinned substrates (For Example: See Figure 4, Column 4 Lines 57-67, Column 5 Lines 8-13, Column 6 Lines 12-17 and Column 12 Lines 5-8); and

c) conductive paths formed between said first of said at least one additional thinned substrate and said second substrate and also between each additional thinned substrate and the directly adjacent additional substrate (For Example: See Figure 4, Column 4 Lines 57-67, Column 5 Lines 8-13 and Column 6 Lines 12-17).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 106-108 and 111-114 are rejected under 35 U.S.C. 103(a) as obvious over Faris (U.S. Patent No. 5,786,629) in view of Sakui et al. (U.S. Patent No. 5,615,163).

In regards to claim 106, Faris discloses the following:

a) at least one controller substrate having logic circuitry formed thereon (For Example: See Column 3 Lines 60-63, Column 7 Lines 8-13 and Column 12 Lines 5-10); and

b) at least one memory substrate having memory circuitry formed thereon (For Example: See Column 3 Lines 60-63, Column 7 Lines 8-13 and Column 12 Lines 5-10).

In regards to claim 106, Faris fails to disclose the following:

a) a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines.

However, Sakui et al. ("Sakui") discloses a plurality of data lines and a plurality of gate lines on each memory substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couple the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines (For Example: See Figure 10, Column 5 Lines 20-67 and Column 6 Lines 1-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include a plurality of data lines and a plurality of gate lines on each memory

substrate and an array of memory cells on each memory substrate wherein memory cells store a data value and have circuitry that couples the data value to one of the plurality of data lines in response to selecting one of the plurality of gate lines as disclosed in Sakui because it aids in providing a means for saving the efficiency of a defective bit (For Example: See Column 5 Lines 11-18 and Column 6 Lines 40-63).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

b) a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment.

However, Sakui discloses a gate line selection circuit (22, 23, 24 and 22') that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one gate line of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

c) controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

However, Sakui discloses controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

In regards to claim 107, Faris fails to disclose the following:

a) the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include that the controller substrate logic tests the array of memory cells periodically to determine if one of the array of memory cells is defective and removes references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

In regards to claim 108, Faris fails to disclose the following:

a) programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines.

However, Sakui discloses programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective memory cells to couple data values to the plurality of data lines (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected defective

memory cells to couple data values to the plurality of data lines as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

In regards to claim 111, Faris fails to disclose the following:

a) logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells.

However, Sakui discloses logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include logic circuitry of the at least one controller substrate that performs functional testing of a substantial portion of the array of memory cells as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

In regards to claim 112, Faris fails to disclose the following:

a) the controller substrate logic is further configured to: prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line (For Example: See Figure 10 and Brief Summary Text). It would have been

obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

In regards to claim 113, Faris fails to disclose the following:

a) the controller substrate logic is further configured to prevent the use of at least one defective gate line.

However, Sakui discloses that the controller substrate logic is further configured to prevent the use of at least one defective gate line (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include that the controller substrate logic is further configured to prevent the use of at least one defective gate line as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

In regards to claim 114, Faris fails to disclose the following:

a) the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate.

However, Sakui discloses that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate (For Example: See Figure 10 and Brief Summary Text). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Faris to include that the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate as disclosed in Sakui because it aids in providing a means for saving a defective bit (For Example: See Column 6 Lines 20-50).

Additionally, since Faris and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Faris.

10. Claim 109 is rejected under 35 U.S.C. 103(a) as obvious over Faris (U.S. Patent No. 5,786,629) in view of Daberko (U.S. Patent No. 5,787,445).

In regards to claim 109, Faris fails to disclose the following:

a) the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell.

However, Daberko discloses that the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell (For Example: See Abstract, Column 3 Lines 66 and 67, Column 4 Lines 1-11, Column 5 Lines 63-67 and Column 6 Lines 1-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Daberko to include that an array of memory cells are arranged within physical space in a

physical order and are arranged within an address space in a logical order and wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell as disclosed in Daberko because it aids in providing direct manipulation of data segments (For Example: See Column 3 Lines 60-64).

Additionally, since Faris and Daberko are both from the same field of endeavor, the purpose disclosed by Daberko would have been recognized in the pertinent art of Faris.

Allowable Subject Matter

11. Claim 110 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
August 16, 2005

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